

5       **METHOD OF IMPROVED HIGH K DIELECTRIC - POLYSILICON INTERFACE  
FOR CMOS DEVICES**

**FIELD OF THE INVENTION**

10       The present invention relates generally to semiconductor fabrication and, more particularly,  
to dielectric layers used in semiconductor fabrication, and to methods of forming capacitors and  
semiconductor circuit components.

**BACKGROUND OF THE INVENTION**

15       The continuing trend in integrated circuits toward densification has led to reduced device  
dimensions and a decrease in size of components that make up the devices. However, in the  
fabrication of such devices as MOS transistors (metal-oxide semiconductors, or MIS or metal-  
insulating semiconductors), and with the trend toward higher performance and processing speeds,  
storage cells must maintain a minimum storage charge to ensure operation of memory cells. Several  
techniques have been developed to increase the storage capacity of a capacitor within a limited  
20       space. For example, surface area has been increased by forming the capacitor in a trench or as a  
stacked structure. The surface area of the capacitor has also been achieved by increasing the surface  
roughness of the lower electrode that forms the storage node.

25       Other techniques concentrate on the use of dielectric materials having high dielectric  
constants (k). Such materials include tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ), titanium dioxide ( $\text{TiO}_2$ ), and  
barium strontium titanate (BST). Such materials effectively possess dielectric constants greater than  
conventional dielectrics (e.g., silicon oxides and nitrides). Due to the high dielectric constant of  
 $\text{Ta}_2\text{O}_5$  and other high K dielectrics, a thicker dielectric layer can be used in capacitor constructions to  
achieve the same capacitance level as thinner layers of other lower K dielectric materials, thus  
reducing cell leakage for the same effective oxide thickness (EOT).

30       Despite the advantages of high dielectric constant materials, difficulties have been  
encountered, however, in incorporating insulating inorganic metal oxide materials into  
semiconductor fabrications. Typically, the deposition of the dielectric layer and a subsequent anneal

to densify the high K dielectric material to reduce leakage is conducted in the presence of an oxygen ambient. Undesirably, the oxygen ambient will react with the underlying lower capacitor plate, typically conductively doped polysilicon, to form a layer of silicon dioxide over the polysilicon that reduces the overall dielectric constant and thereby reduces the cell capacitance.

5 One solution that has been utilized is to provide an intervening oxidation barrier layer between the inorganic metal oxide dielectric layer and the underlying polysilicon electrode. Present methods include forming a silicon nitride layer over the polysilicon prior to formation of the Ta<sub>2</sub>O<sub>5</sub> or other dielectric layer, by rapid thermal nitridization (RTN) of the polysilicon electrode. The nitride layer is used to reduce the oxidation of the lower polysilicon electrode during the deposition  
10 of the dielectric layer and subsequent oxidation and conditioning treatments. The subsequent treatment processes invariably oxidize the underlying polysilicon electrode to reduce the leakage of the dielectric-polysilicon stack. However, the overall capacitance is undesirably reduced due to the physical thickness of the subsequent oxynitride layer, which is typically up to 30 angstroms.

Thus, a need exists for a process for integrating high dielectric constant materials into  
15 semiconductor devices that avoids such problems.

### **SUMMARY OF THE INVENTION**

The present invention provides methods for forming dielectric layers over polysilicon substrates and in the construction of semiconductor devices, methods for forming capacitors and  
20 other semiconductor devices, and semiconductor devices and capacitor structures.

It is recognized that the lower polysilicon electrode of a capacitor construction should become oxidized to some degree during processing for reduction of cell leakage. The present invention utilizes a self-limiting oxynitride layer to achieve polysilicon oxidation, and as an interface layer prior to deposition of Ta<sub>2</sub>O<sub>5</sub> or other dielectric layer. The process flow of the invention  
25 utilizing a self-limiting nitric oxide (NO) anneal of the polysilicon layer at less than 800°C to grow a thin oxide (oxynitride) layer of about 40 angstroms or less, preferably less than 15 angstroms, over the polysilicon layer. The anneal results in the formation of a layer of nitrogen at the polysilicon-oxide interface that inhibits oxygen diffusion through the oxide layer to the underlying polysilicon, thus inhibiting further oxidation of the polysilicon layer and additional growth of the

oxide layer. The oxide layer is then annealed, preferably plasma annealed, in a nitrogen-containing ambient to nitridize the surface of the oxide layer, resulting in layer of silicon nitride ( $\text{SiN}_x$ ) formed over the oxide layer. The silicon nitride layer reduces the effective dielectric constant of the oxide layer.

Advantageously, the thickness of an oxide layer grown over polysilicon with nitric oxide and overlain with tantalum pentoxide or other high K dielectric that is subsequently reoxidized is less than the thickness of an oxide layer grown over polysilicon by conventional RTN with a reoxidized high K dielectric layer. By use of the present invention, a post-treatment oxidation anneal of a high K dielectric layer will not oxidize the underlying polysilicon layer to any substantial degree.

In addition, the process of the invention results in reduced electrical thickness of the interface layer in a capacitor construction, and thus increased capacitance without adversely affecting the leakage (defectivity) of the stack. The present process achieves more capacitance with the same or reduced leakage (cell defects). The process further provides reduced Dt of the entire process flow by replacing the conventional  $750^\circ\text{C}$  anneal in nitrous oxide ( $\text{N}_2\text{O}$ ) for crystallization of the dielectric (e.g.,  $\text{Ta}_2\text{O}_5$ ) layer with a shorter 700 to  $750^\circ\text{C}$  anneal of the polysilicon layer in nitric oxide (NO).

In one aspect, the invention provides methods for forming a dielectric layer over a polysilicon substrate. The polysilicon substrate is annealed in nitric oxide (NO) to form an oxide (oxynitride) layer, the oxide layer is nitridized to form a nitride layer, and the dielectric layer is deposited onto the nitride layer. In one embodiment of the method, the polysilicon substrate such as HSG polysilicon, is annealed in nitric oxide at a temperature of less than  $800^\circ\text{C}$ ., preferably about  $700^\circ\text{C}$ . to about  $750^\circ\text{C}$ . to form an oxynitride layer, preferably an active nitrogen-containing species formed in a plasma, of about 40 angstroms or less, preferably less than 15 angstroms. The oxynitride layer is then exposed to a nitrogen-containing gas, preferably a plasma source of nitrogen, to form a silicon nitride layer over the surface. A high K dielectric layer such as tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) is then formed over the nitride layer, and annealed in an oxidizing gas. The thickness of the oxynitride layer remains substantially the same as before the oxidizing anneal of the dielectric layer.

In another aspect, the invention provides methods for forming a semiconductor device above a semiconducting substrate. In one embodiment of the method, an oxynitride layer is formed over a polysilicon substrate by annealing the polysilicon substrate in the presence of a nitric oxide,

preferably at a temperature of less than 800°C. to form an oxide layer of about 40 angstroms or less with a preferred thickness of less than 15 angstroms; nitridizing the oxide layer in a nitrogen-containing gas; and forming a dielectric layer over the nitrided surface of the oxide layer, preferably with a high K dielectric such as tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) which is then subjected to an oxidizing anneal to condition the material.

In yet another aspect, the invention provides methods for forming a capacitor. In one embodiment of the method, a first capacitor electrode comprising polysilicon is formed over a substrate, an oxide (oxynitride) layer is grown over the first capacitor electrode by annealing the electrode in the presence of a nitric oxide, preferably at a temperature of less than 800°C., to a thickness of about 40 angstroms or less, with a preferred thickness of less than 15 angstroms; the oxide layer is exposed to a nitrogen-containing gas to form a nitride layer over the surface; and a dielectric layer is formed over the nitride layer, preferably using a high K dielectric such as tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) which is then annealed in an oxidizing gas. A conductive second capacitor electrode can then be formed over the dielectric layer.

In another embodiment, a capacitor can be formed by providing a substrate comprising an overlying insulative layer and a container opening formed in the insulating layer to an active area on the substrate and a lower electrode comprising polysilicon formed within the container opening; growing an oxide (oxynitride) layer over the lower electrode to a thickness of about 40 angstroms or less, with a preferred thickness of less than 15 angstroms, by annealing the polysilicon electrode in the presence of nitric oxide; nitridizing the oxide layer in a nitrogen-containing gas; and forming a layer of a dielectric material, preferably a high K dielectric, over the nitridized oxide layer. A conductive upper electrode can then be formed over the dielectric layer.

In another aspect, the invention provides a semiconductor device. In one embodiment, the device comprises an oxynitride layer overlying a polysilicon substrate, the oxynitride layer comprising a nitric oxide grown oxide layer of up to about 40 angstroms, with a preferred thickness of less than 15 angstroms; a layer of silicon nitride overlying the oxynitride layer; and a layer of a dielectric material, preferably a high K dielectric that has been oxygen annealed, overlying the nitride layer.

In yet another aspect, the invention provides a capacitor. In one embodiment, the capacitor comprises a first conductive capacitor plate comprising polysilicon; a thin oxynitride layer overlying the first capacitor plate, the oxynitride layer comprising an oxide layer grown in the presence of nitric oxide, having a thickness of about 40 angstroms or less, preferably less than 15 angstroms; a layer of silicon nitride overlying the oxynitride layer; and a dielectric layer overlying the nitride layer, preferably comprising an oxygen annealed high K dielectric material. Additionally, the capacitor can comprise a second conductive capacitor plate overlying the dielectric layer.

In another embodiment, the capacitor can comprise a container formed in an insulative material such as BPSG, and a lower capacitor electrode comprising polysilicon such as HSG polysilicon formed in the container; an oxide (oxynitride) layer overlying the lower capacitor electrode, and comprising nitric oxide grown oxide of about 40 angstroms or less, preferably less than 15 angstroms thick; a silicon nitride layer over the surface of the oxide layer; and a dielectric layer, preferably an oxidized high K dielectric, overlying the nitride layer. The capacitor can further comprise an upper capacitor electrode overlying the dielectric layer.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

Preferred embodiments of the invention are described below with reference to the following accompanying drawings, which are for illustrative purposes only. Throughout the following views, the reference numerals will be used in the drawings, and the same reference numerals will be used throughout the several views and in the description to indicate same or like parts.

**FIG. 1A** is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary step of a processing sequence.

**FIGS. 2-5** are views of the wafer fragment of **FIG. 1** at subsequent and sequential processing steps, showing fabrication of an capacitor according to an embodiment of the method of the invention.

### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

The invention will be described generally with reference to the drawings for the purpose of illustrating the present preferred embodiments only and not for purposes of limiting the same. The

figures illustrate processing steps for use in the fabrication of semiconductor devices in accordance with the present invention. It should be readily apparent that the processing steps are only a portion of the entire fabrication process.

In the current application, the terms “semiconductive wafer fragment” or “wafer fragment” or “wafer” will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term “substrate” refers to any supporting structure including, but not limited to, the semiconductive wafer fragments or wafers described above.

An embodiment of a method of the present invention is described with reference to **FIGS. 1-5**, in a method of forming a dielectric layer in the construction of a container capacitor. While the concepts of the invention are conducive to the fabrication of container capacitors, the concepts described herein can be applied to other semiconductor devices that would likewise benefit from the fabrication of a dielectric film as described herein. Therefore, the depiction of the invention in reference to the manufacture of a container capacitor is not meant to limit the extent to which one skilled in the art might apply the concepts taught herein.

Referring to **FIG. 1**, a portion of a semiconductor wafer 10 is shown at a preliminary processing step. The wafer fragment 10 in progress can comprise a semiconductor wafer substrate or the wafer along with various process layers formed thereon, including one or more semiconductor layers or other formations, and active or operable portions of semiconductor devices.

The wafer fragment 10 is shown as comprising a substrate 12 and an overlying insulation layer 14. An exemplary substrate 12 is monocrystalline silicon that is lightly doped with a conductivity enhancing material. Exemplary insulation materials include silicon dioxide ( $\text{SiO}_2$ ), phosphosilicate glass (PSG), borosilicate glass (BSG), and borophosphosilicate glass (BPSG), in a single layer or multiple layers, with the insulation layer 14, being BPSG in the illustrated example. A container or opening 16 has been conventionally etched into the BPSG insulation layer 14.

An electrically conductive material forms a lower capacitor electrode layer 18 that has been formed on the insulative substrate 14 within the opening 16. The electrode layer 18 comprises a

semiconductive material such as HSG polysilicon, and undoped or conductively doped polysilicon, being HSG polysilicon in the illustrated example. The electrode layer 18 can be formed by conventional fabrication methods known and used in the art.

Referring now to **FIG. 2**, a thin oxide (oxynitride) layer 20 is thermally grown over the polysilicon electrode layer 18 using a self-limiting anneal of the electrode layer 18 in nitric oxide (NO) gas. As the oxide layer 20 builds up, the underlying polysilicon electrode layer 18 is no longer oxidizable and the nitric oxide ambient thus becomes a self-limiting oxidation ambient. The annealing localizes nitrogen near the interface 19 between the polysilicon layer 18 and the oxide layer 20. The resulting thin nitrogen layer at the polysilicon-oxide interface inhibits diffusion of oxygen through the oxide layer 20 into the underlying polysilicon layer 18, thus preventing further oxidation of the polysilicon layer during subsequent processing steps, i.e., a post-RPN (plasma anneal). A preferred technique for forming the oxide layer 20 is to expose the polysilicon layer 18 to nitric oxide (NO) gas at a temperature of less than 800°C., preferably about 700 to about 750°C., for about 1 to about 3600 seconds, at about 1 mTorr to greater than atmospheric pressure, preferably atmospheric pressure, to grow a thin oxide layer 20 that is about 40 angstroms or less, and preferably less than 15 angstroms.

The oxide layer 20 is then exposed to a plasma generated nitrogen species to form a nitrogen-containing layer 24, as shown in **FIG. 3**. The nitride layer 24 on the surface of the oxide layer 20 reduces the effective dielectric constant of the oxide layer 20. Preferably, the nitride layer 24 is about 5 to about 15 angstroms thick, preferably about 10 angstroms, and the oxide layer 20 and the nitride layer 24 collectively have a physical thickness of about 10 to about 40 angstroms, preferably about 10 to about 30 angstroms, preferably about 15 angstroms.

The nitridizing process step can occur in a rapid thermal processor or, preferably, a plasma reactor such as a high density plasma reactor or remote plasma chamber, typically over a temperature range of about 0 C. to about 900°C. Exemplary nitrogen-containing gases include nitrogen (N<sub>2</sub>), ammonia (NH<sub>3</sub>), nitrogen (N<sub>2</sub>) with helium (He), nitrogen (N<sub>2</sub>) with argon (Ar), nitrogen oxides (NO<sub>x</sub>) including nitrous oxide and nitric oxide, and mixtures thereof.

A preferred nitridization process comprises exposing the wafer 10 to an remote plasma source of nitrogen, preferably a microwave source, at a temperature of about 350 to about 900°C, a

pressure of about 1mTorr to about 100 Torr, preferably about 1 to about 10 Torr, with a microwave generated plasma in nitrogen (N<sub>2</sub>) and helium at a He:N ratio of about 4:1, and at a flow rate of the nitrogen-containing gas of about 1 to about 5000 sccm, for about 1 to 1800 seconds.

Following nitridization, a dielectric layer 26 is then formed over the nitride layer 24, as depicted in **FIG. 4**, according to techniques known and used in the art. Preferably, the dielectric layer 26 comprises a high dielectric constant (high K) material. "High K" materials are to be distinguished from conventional dielectric materials such as silicon dioxide (k~3.9). Examples of high K materials for dielectric layer 26 include tantalum pentoxide (Ta<sub>2</sub>O<sub>5</sub>), titanium dioxide (TiO<sub>2</sub>), barium strontium titanate (BST), strontium titanate (ST), barium titanate (BT), lead zirconium titanate (PZT), strontium bismuth tantalate (SBT), hafnium oxide (HfO<sub>2</sub>), zirconium oxide (ZrO<sub>2</sub>), and aluminum oxide (Al<sub>2</sub>O<sub>3</sub>), being Ta<sub>2</sub>O<sub>5</sub> in the illustrated example. The dielectric layer 26 can be formed by a variety of techniques known and use in the art such as low pressure chemical vapor deposition (LPCVD), remote plasma deposition, among other techniques.

Subsequently, the high K (Ta<sub>2</sub>O<sub>5</sub>) layer 26 can be subjected to post-treatment processing to reduce leakage and improve its dielectric qualities by saturating the layer 26 with oxygen. Typically, Ta<sub>2</sub>O<sub>5</sub> is subjected to an anneal in the presence of an oxidizing gas. The oxygen anneal is typically conducted utilizing one or more of oxygen (O<sub>2</sub>), plasma oxygen, ozone (O<sub>3</sub>) and nitrous oxide (N<sub>2</sub>O), with or without plasma excitation.

In a conventional process flow, post-treatment processing of the dielectric layer 26 in an oxygen ambient would undesirably oxidize the underlying polysilicon layer 18. However, the presence of the oxide layer 20 and the silicon oxynitride layer 24 according to the invention, provides the benefit of providing a nitrogen barrier to diffusion of oxygen through the oxide layer 20 to the polysilicon layer 18 during post treatment oxidation of the dielectric layer 26.

Referring now **FIG. 5**, a conductive material is then deposited over the dielectric layer 26 to form the top capacitor electrode (plate) 28 and complete the capacitor structure. The top electrode 28 can be formed by conventional techniques from a conductive material such as doped polysilicon or a conductive metal such as tungsten, tungsten nitride, titanium nitride, and platinum. The conductive material can be deposited on the dielectric layer 26 by conventional methods, such as



CVD, or physical vapor deposition (e.g., sputtering) for a metal plate, to complete the capacitor structure.

5 In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

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